REMARKS

Claims 24-38, all the claims pending in the application, stand rejected on prior art grounds.

I. The Prior Art Rejections

Claims 24-29, 31-35, and 37-38 stand rejected under 35 U.S.C. §102(b) as being anticipated by Lee et al., hereinafter "Lee", and claims 30 and 36 stand rejected under 35 U.S.C.§ 103(a) as being unpatentable over Lee in view of Akatsu et al., hereinafter "Akatsu". Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Lee

The Office Action argues that Lee discloses that the gate material of both the bottom and top gates is polysilicon and that the spacer is silicon oxide and that, therefore, the spacer material is independent of the material of the top and bottom gate. However, Lee teaches that the gate sidewalls should be an oxide growth, which requires that the sidewalls comprise an oxidized form of the gate material. Thus, with Lee, the gate sidewall spacers are dependent upon the material of the gate itself and Lee does not teach that "said spacers comprise a material that is independent of the material of said top gate and said bottom gate" as defined by independent claim 24.

The Office Action states that in Lee, the gate material is a polysilicon while the spacer is silicon oxide. This statement demonstrates that the spacer material in Lee is not independent of the gate material because both are silicon based. Following the teachings of Lee requires that the spacers be an oxide of the gate material and therefore, the spacers must be dependent upon the gate material. To the contrary, with the claimed invention, the spacer material could comprise any insulator (such as a deposited insulator), while the gate material could comprise any form of conductor such as a metal, polysilicon, etc.

The last five lines of the first column of page 3.5.1 of Lee explain that by utilizing the oxidation rate difference between the two poly gates and the lightly doped channel region, Lee can grow a much thicker isolation oxide on the side wall of the poly gates, as shown in Figure (d) of Lee. This gives the structure in Lee the unique shape where the isolation oxide is thicker adjacent the upper and lower gates and is narrower near the channel region silicon film. Therefore, the disclosure in Lee requires that the spacers adjacent the gate conductors be an oxide of the gate material. Thus, Lee requires that the spacers be depended upon the material makeup of the upper and lower gates. This is directly contrary to the claimed invention where "said spacers comprise a material that is independent of the material of said top gate and said bottom gate" as defined by independent claim 24.

Because the inventive process uses the sacrificial nitride layers 310, 312, 305 and replaces the sacrificial layers with the upper and lower gates 502, 503, the material selection for the spacers 314, 307 is completely independent of the material selection of the upper and lower gates 502, 503. To the contrary, the structure disclosed in Lee is most clearly seen in Figure 1f which illustrates a top gate and a bottom gate separated by a channel region, with a continuous oxide separating the gates from the source and drain regions.

As shown in Applicants' Figure 11, because the inventive process forms the spacers 307, 1200 that are adjacent to the top gate 502 in separate processing steps, the inventive structure includes distinct upper and lower spacers adjacent the top gate. The Office Action argues that Figure (e) of Lee discloses the difference spacers adjacent the upper gate. The only structures in Figure (e) of Lee that have some difference in the vicinity of the upper gate appear to be the selective epitaxy regions. However, these selective epitaxy regions are not adjacent to the gate in Lee, but instead the uniform oxide spacers are adjacent the upper gate in Lee. Therefore, it is improper to equate the claimed spacers with the selective epitaxy described in Figure (e) of Lee. To the contrary, Lee only discloses a single continuous oxide spacer adjacent the top gate. Thus, Lee cannot teach or suggest "spacers in direct contact with said top gate, wherein said spacers comprise lower spacers in direct contact with a lower section of said top gate and upper spacers in direct contact with an upper section of said top gate" as defined by independent claims 29 and 35.

Further, because the invention utilizes a self aligned silicide process, the inventive structure includes silicide regions 1300 that are adjacent the point where the upper spacers 1200 and the lower spacers 307 meet. Once again, because Lee teaches a single continuous spacer along the sidewalls of the top gate, it cannot teach or suggest claimed invention where "said silicide regions are adjacent a point where said upper spacers meet said lower spacers" as defined by independent claim 35.

Therefore, as shown above, the applied prior art reference Lee does not teach or suggest the invention defined by independent claims 24, 29, and 35. Therefore, the independent claims (and the dependent claims 25-28, 30-34, and 36-38 by their dependency) are patentable over Lee. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. The Rejection Based on Lee in view of Akatsu

Applicants respectfully traverse the rejection based upon Lee and Akatsu principally because Akatsu is directed to a single gate transistor as opposed to the double gate transistors defined by Applicants' claims and disclosed by Lee. One ordinarily skilled in the art would not have made reference to Akatsu when forming a double gate transistor. More specifically, the Office Action proposes that Akatsu discloses that the spacers adjacent upper and lower portions of the gate can comprise different materials. However, Akatsu cannot teach or suggest any feature regarding the upper gate of a double gate transistor because Akatsu only includes a single gate stack and does not provide any teaching regarding what type of spacers could be utilized next to the upper gate of a double gate transistor structure. Therefore, Applicants initially traverse this rejection because a prima facia case of obviousness has not been set forth in that one ordinarily skilled in the art will not have made reference to Akatsu when preparing a double gate transistor structure.

Further, Applicants note that Akatsu teaches a gate stack that includes multiple layers of conductors (polysilicon 18, gate conductor 20) where a first type of material (oxide 26 shown in Figure 1) is used adjacent to the lower portion of the gate stack 18 and a different type of material

(nitride 24) is used adjacent the next conductive layer 20 within the gate stack. Applicants submit that these different types of insulators taught by Akatsu are utilized because the different materials used within the gate stack would require the use of different sidewall spacers. To the contrary, with the invention, the different spacers are adjacent to a single upper gate (which is different than the gate stack that includes multiple layers of conductors in Akatsu). Therefore, Akatsu would not teach or suggest to one ordinarily skilled in the art to use different materials as sidewall insulators along a uniform gate material as in the claimed invention. Thus, it is also Applicants position that even if one ordinarily skilled in the art had combined Akatsu and Lee, the proposed combination would not teach or suggest that the "lower spacers comprises a different material than said upper spacers" as defined by dependent claims 30 and 36. Therefore, it is Applicants' position that dependent claims 30 and 36 are patentable over the prior art of record. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 24-38, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

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Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 50-0510.

Respectfully submitted,

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